## REMARKS

Applicant thanks the Examiner for indicating that claims 5-13, 16 and 17 contain allowable subject matter.

Applicants respectfully request reconsideration of claims 1-3, 14 and 15, as amended, as set forth below.

### I. Amendment

Claim 1 has been amended to more particularly point out the invention therein. Claims 18 and 19 are newly added.

No new matter has been added.

### II. Prior Art Rejections

Claims 1, 2, 3, 14 and 15 stand rejected under 35 U.S.C. §103 as being unpatentable over the combination of Yoshida (U.S. Patent 5,998,843) and Wolf, SILICON PROCESSING FOR THE VLSI ERA, Vol. 2, Process Integration, as set forth on pages 2-3 of the Office action.

Obviousness can only be established by combining or modifying the teachings of the prior art to ***produce the claimed invention*** where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *Ecolochem Inc. v. Southern California Edison Co.*, 227 F.3rd 1361, 56 U.S.P.Q.2d (BNA) 1065 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2D (BNA) 1614, 1617 (Fed. Cir. 1999); *In re Jones*, 958 F.2d 347, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992); and *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). See also MPEP 2143.01.

Neither Yoshida nor Wolf, taken alone or in combination, disclose or suggest a semiconductor device which includes a source/drain diffused layer formed in the substrate for a transistor; a first shallow trench isolation formed in the substrate; a second shallow trench isolation formed in the substrate; and a dummy diffused layer formed between the first and second shallow trench isolations, wherein the source/drain diffused layer has its surface silicided, and the dummy diffused layer has its surface covered with an anti-silicidation film at least partially, on which no gate electrode is provided, as recited by amended claim 1. Yoshida discloses to use a p-type well region 7 between a PMOS region and a Bipolar region. Fig. 10. The p-type well region 7 has field oxide film 5 formed thereon. Yoshida does not disclose or suggest a semiconductor device as recited in amended claim 1 including a dummy diffused layer formed between a first and second shallow trench isolation. Likewise, although Wolf discloses various techniques for forming insulating layers, Wolf also does not disclose or suggest a semiconductor device as recited in amended claim 1 including a dummy diffused layer formed between a first and second shallow trench isolation.

As neither Yoshida nor Wolf, taken alone or in combination, disclose or suggest all of the limitations of amended claim 1, the combination of the Yoshida and Wolf, even if considered proper, *arguendo*, does not produce the claimed invention. Hence, neither Yoshida nor Wolf, taken alone or in combination, render claim 1, nor claims 2, 3, 14 and 15 which depend on claim 1 and incorporate all of the limitations thereof, unpatentable.

**III. New Claims 18 and 19**

New claim 18 and 19 depend on claim 1 and are allowable at least for the same reasons as claim 1.

It is further noted that applicant respectfully submitted that new claims 18 and 19 recite novel feature(s) which are believed to provide an additional basis for patentability over Yoshida and the Wolf.

For example, claim 18 recites, in a pertinent part, "the dummy diffused layer is formed so as to prevent dishing". Applicants note that a shallow trench isolation (STI) region with a large area may be subjected to "dishing" (i.e. its height may decrease by a level difference as illustrated in Fig. 16D of the present invention) during a CMP step. The dummy diffused layer in claim 18 is adopted to prevent dishing (see page 4, line 7 – page 6, line 5). However, in Yoshida, the isolation structure 5 is a LOCOS isolation rather than a shallow trench isolation. Accordingly, Yoshida does not face the problem of dishing and would not be motivated to place the dummy diffused layer so as to prevent dishing.

Claim 19 recites "no transistor is formed between the first shallow trench isolation and the second shallow trench isolation". Turning to Yoshida, a transistor is formed between the isolation structures which locate both side of examiner alleged dummy diffused layer.

## IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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